Amendments to the Specification:

Please replace the paragraph starting on p. 10, line 8 with the following amended paragraph:

A1

Referring now to Figure 1, a first embodiment of a bit disparity monitor 100 is shown in detail. The bit disparity monitor 100 may be a component of an optical transmitter which may form part of a node in an optical network such as SONET or a wavelength division multiplexing (WDM) system. The bit disparity monitor 100 comprises a sub-sampler 105, a clock generator 110, a 1's detector 115, a 1's counter 120, a timer 125, a samples counter 130, a comparator 135 and a memory 140.

Please replace the paragraph starting on p. 11, line 14 with the following amended paragraph:

A2

The timer 125 also generates a periodic timer signal at a rate which is lower than the clock rate and transmits it along control line 126 to the 1's ~~detector 115~~ counter 120 and along control line 127 to the samples counter 130. In a preferred embodiment, it in fact generates periodic timer signals upon expiry of the timer at a plurality of periods, typically a low, medium and long time period.

Please replace the paragraph starting on p. 16, line 1 with the following amended paragraph:

A3

The inverted data sub-sampler 310 accepts as input the inverted signal generated by the signal inverter 305 along transmission line 306 and a clock signal from the clock generator 110 along control line 307. It outputs a sub-sampled data stream of the input inverted signal along control line ~~211~~ 311 to the 0's detector ~~215~~ 315. The input inverted signal is sub-sampled at each instance of the clock signal received from the clock generator 110, which drives the sub-sampling of the non-inverted signal by the sub-sampler 105.